REMARKS

Claims 1 to 44 were pending in the application at the time of issuance of the office action. Claims 1 to 7, 9 to 12, 14, 15 to 18, 20 to 28, 30 to 34, 36, 37, 39, 40, 42 and 44 remain rejected as anticipated. Claims 8, 13, 29, 35, 38, 41 and 43 remain rejected under 35 U.S.C. 103(a).

The amendment to the specification corrects a typographical error.

Applicants have further amended Claims 1, 9, and 15. The amendments are supported, for example, at least by Figs. 3 and 4 and the description thereof. The amendments make explicit how the aliasing is accomplished, the inputs, the outputs and the entries in the various structures. Claim 33 is amended to correct a grammatical informality.

Claims 1 to 7, 9 to 12, 14, 15 to 18, 20 to 28, 30 to 34, 36, 37, 39, 40, 42 and 44 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,996,071, hereinafter referred to as White.

Applicants respectfully traverse the anticipation rejection of Claim 1 and the reliance on the L1 cache, which goes against the express teaching of White. White first taught:

> FIG. 6a illustrates the Branch Unit (BU) 250, which includes the branch target cache (BTC) 252, a return stack (RSTK) 342, and a branch resolution buffer (BRB) 344. The BU stores target information used for prefetching target addresses both (a) for conditional COFs (branches), i.e., JCC and LOOPs, and (b) for unconditional COFs (UCOFs), i.e., JMPs (jump) and CALLs/RETurns.

White, Col. 16, line 66 to. Col. 17, line 5. Thus, White expressly taught that the Branch Unit, and not the L1 cache, stored target information used for prefetching target addresses for branches.

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White further taught:

> In particular, the BTC stores only the L1 Cache index [11:4] portion of the target address, but not the corresponding cache tag [31:12] portion. A prefetch access with the L1 Cache index will enable set selection to be performed, but the cache tag will not be available for tag comparison to select the way in which the cache line containing the target instruction is stored--instead, the way number cached in the BTC along with the L1 Cache index is used for way selection, allowing the L1 Cache to return a cache line in response to the prefetch request.

White, Col. 18, lines 25 to 34.

White expressly describes how information in the branch target cache is provided to the L1 Cache so that the L1 cache can return a cache line in response to the prefetch request. The output cache line from the L1 cache is described as "the prefetch block of instruction bytes returned to the Prefetch Unit." White, Col. 18, lines 3 and 4. Thus, the L1 cache holds the target instruction that is executed based on the prediction by the branch unit as to what instruction should be executed next and fails to have any input on determining the direction of the branch or any branch qualifier. White makes it clear that it is the branch unit and not the L1 cache that makes the determination of the predicted path.

As noted in the rejection, White taught:

> For conditional COFs that hit in the BTC 252, the predicted path depends on the history information stored along with the target information for that entry.

White, Col. 17, lines 34 to 36.

Thus, contrary to the rejection, the predicted path is not determined using information in the L1 cache, but instead White expressly stated that the history information and the branch target information, shown in Fig. 6c of White, were used. White makes this even clearer:

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> For the exemplary BTC, the target information used for prefetching target prefetch blocks containing target instructions is the L1 Cache index and way number that together define a particular cache location (containing a prefetch block cache line)

White, Col. 17, lines 50 to 53. Thus, the target information is in the BTC and is used to prefetch target instruction in the L1 cache. Again, the branch prediction is expressly stated as being based on information in the branch target cache and not information in the L1 cache.

Thus, as best the rejection is understood, the branch target cache (BTC) of White is being taken as teaching Applicants' invention, where the branch target information in the cache including the way and set number is taken as a branch direction indication. Apparently, the history information in the BTC of White is taken as a branch qualifier indication.

However, this teaches away from Applicants' invention. White taught the each entry, as shown in Fig. 6c, of the BTC included:

> Each BTC entry includes bits [11:0] of the target address comprising (a) a set number [11:4] formed by the L1 Cache Index, and (b) a byte location number [3:0]. The L1 cache index [11:4], together with a 2 bit way number, identify a particular cache location (set and way) assumed to store the prefetch block containing target instruction--the byte number identifies 1 of 16 bytes that is the initial target instruction byte.
>
> Finally, each entry includes a valid bit, a three-bit IB__LOC field that designates the IB buffer location for short COFs, branch history bits, and two attribute bits PWT (page write through) and PCD (page cache disable).

Thus, White taught that each entry included both the history bits and the branch target information. This fails to teach or suggest aliasing the history bits so that the number of history bit entries is less than the number of branch target information entries in the BTC. Accordingly, White fails to

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teach the invention in the same level of detail as recited in Claim 1. Applicants request reconsideration and withdrawal of the anticipation rejection of Claim 1.

Each of independent Claims 9, 15, 25, 30, 33 and 39 includes limitations similar or equivalent to those discussed above with respect to Claim 1. Therefore, the remarks with respect to Claim 1 are applicable to each of these claims and are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 9, 15, 25, 30, 33 and 39.

Each of Claims 2 to 7 depends from Claim 1 and so distinguishes over White for at least the same reasons as Claim 1, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 2 to 7.

Each of Claims 10 to 12 and 14 depends from Claim 9 and so distinguishes over White for at least the same reasons as Claim 9, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 10 to 12 and 14.

Each of Claims 16 to 18 and 20 to 24 depends from Claim 15 and so distinguishes over White for at least the same reasons as Claim 15, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 16 to 18 and 20 to 24.

Each of Claims 26 to 28 depends from Claim 25 and so distinguishes over White for at least the same reasons as Claim 25, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 26 to 28.

Each of Claims 31 and 32 depends from Claim 30 and so distinguishes over White for at least the same reasons as

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Claim 30, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 31 and 32.

Each of Claims 34, 36 and 37 depends from Claim 33 and so distinguishes over White for at least the same reasons as Claim 33, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 34, 36 and 37.

Each of Claims 40 and 42 to 44 depends from Claim 39 and so distinguishes over White for at least the same reasons as Claim 39, which reasons are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 40 and 42 to 44.

Claims 8, 13, 29, 35, 38, 41 and 43 stand rejected under 35 U.S.C. 103(a). Assuming that the combination of references is correct for each of these claims, the additional material relied upon from the secondary reference does not correct the deficiencies of White with respect to the independent claims from which these claims depend. Therefore, each of Claims 8, 13, 29, 35, 38, 41 and 43 distinguish over the combination of references for at least the same reasons as the independent claims. Applicants respectfully request reconsideration and withdrawal of the obviousness rejection of each of Claims 8, 13, 29, 35, 38, 41 and 43.

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Claims 1 to 44 remain in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 2, 2007.

Attorney for Applicant(s) — May 2, 2007 Date of Signature

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